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Phison Electronics Corporation

PS8005 Controller Specification

(For SD Card)

version1. 7

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Revision History

Revision	History	Draft Date	Remark
1.1	First Release	2007	Horace
1.3	Modify pin 1,2,17,47,48 description	28-May-07	Carol
1.4	1. Item F. Pin Assignment and Description Modify pin 17,47,49,51 description 2. Item K. Package Information Modify Top view & Bottom view Modify Symbol A,A1,A2,L Remove Symbol L1,L2	06-Jun-07	Carol
1.5	Item K. Package Information(Page. 17) Add Symbol L	11-Jun-07	Carol
1.6	1.Modify IC Technology (Page. 3) 2.Item F. Pin Assignment and Description Modify pin 25 description Correct typing error in PS8002 LGA Top View-pin8 3.Modify Storage Temperature in page10	2-July-07	Carol
1.7	1. Correct typing error in page 2 (High Voltage range) & page 10 (VDD Voltage) & page3(Specifications support) 2. Modify IC technology in page 3.	8-Aug-07	Carol

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A. General Description

Phison's flash memory controller PS8005 is specially designed for the Secure Digital (SD) Card. It allows the selection of either SD or SPI mode. To store and transfer data securely, the PS8005 controller provides both data write protection and password protection. In addition, it has a built-in SRAM Buffer and a Dual Buffer mode to allow smooth reading and writing. Using this one chip solution, both RMA problems and manufacturing time between Research & Development and mass production will be significantly reduced.

PS8005 also extends the clock frequency to 50MHz for higher data transfer rate. Support 2x8 Dual Channel + Interleave operation, The multiple (x1 bit, x4 bit) bus-width feature allows for host design flexibility and higher data transfer bandwidth.

B. Controller Features

- ◆ Support SD system specification version 1.01, 1.1 and 2.0 (High Capacity)
- ◆ Designed for read-only, read/write storage cards.
- ◆ Support SD SPI mode.
- ◆ Block read and block write supported [class 2 and class 4]
- ◆ Erase supported [class 5]
- ◆ Write protection supported [class 6]
- ◆ Lock card supported [class 7]
- ◆ CPRM(Content Protection for Recordable Media) of SD Card supported.
- ◆ Variable clock rate 0 - 50 MHz.
- ◆ High performance flash memory control with dual SRAM buffer mode.
- ◆ Transmission speed :
SD-4bit interface Read / Write : 23 MB/sec (Max) / 20 MB/sec (Max)
SD-1bit interface Read / Write : 3.1 MB/sec (Max) / 2.9 MB/sec (Max)
- ◆ High Voltage range for communication : 2.7 - 3.6V.
- ◆ Dual voltage SD Card : Operating voltage range : Low Voltage Range(T.B.D)
and 2.7-3.6 V
- ◆ Support up to 12bit ECC circuits to protect data communication.

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C. Main Features Guide

Main Features	PS8005
Specifications support	SD2.0 (Backward compatible to 1.x host)
CPRM support	Yes
Lock/unlock function support	Yes
SLC NAND Flash support : Small Block-- Large Block--	No Support 1Gb~64Gb* ¹
MLC NAND Flash support : Small Block-- Large Block--	No Support refer to flash supported list table as below
Maximum Storage Capacity(CSD) support	SD1.01, SD1.1 – up to 2GB SD 2.0 & SDHC 4GB – 32GB
Number of NAND Flash support	Single Channel : 4 Dual Channel : 8
Voltage Supports	Dual Voltage 1.8/3.3V
Flash I/O	8-bit/16-bit* ²
IC Technology	0.162um
Controller Package (mm x mm x mm)	LGA-51pin 3.0 x 7.6 x 0.7

*1 : The DDP/QDP flash type.

*2 : 2x8-bit parallel mode(Dual channel)

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D. Flash Supported Table

D1. Flash type list and definition

SLC	Single-Level Cell
MLC	Multi-Level Cell
SB	Small Block i. 512+16Bytes per page (No support)
LB	Large Block i. 2k+64Bytes per page ii. 4k+128Bytes per page iii. 4K+218Bytes per page

Type	SLC-LB	MLC-LB (Conv.)	MLC-LB (ABL)
Capacity	1Gb	2Gb	1Gb
	2Gb	4Gb	2Gb
	4Gb	8Gb	4Gb
	8Gb	16Gb	8Gb
	16Gb Note1	32Gb	16Gb Note1
		64Gb Note1	
Vendor	Hynix, Intel, Micron, Samsung, ST, Toshiba	Hynix, Intel, Micron, Samsung, ST, Toshiba	Toshiba

Note1 : There was DDP/QDP flash type.

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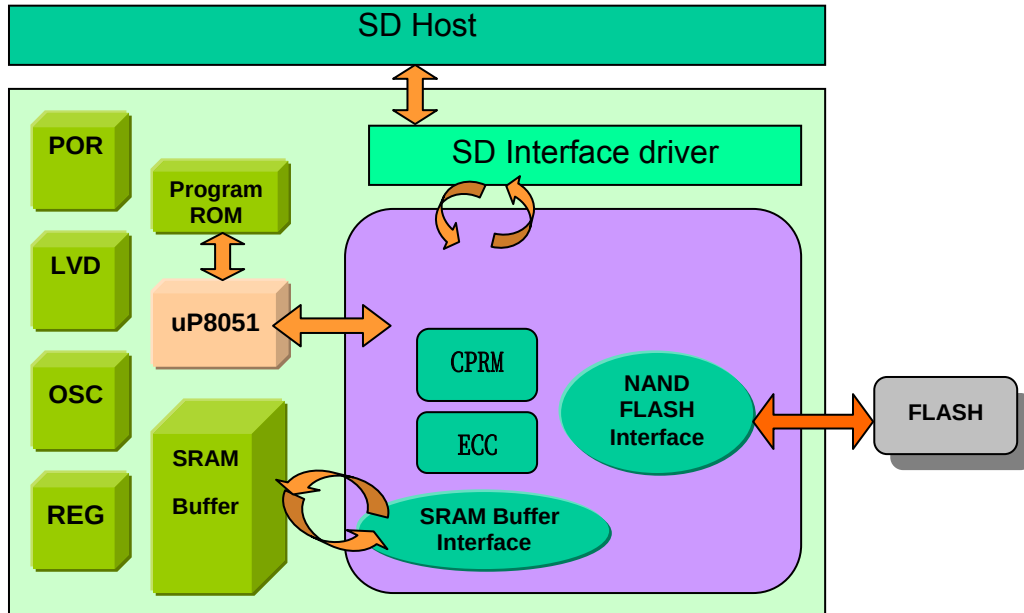
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D2. Flash supported table

F/W ver.		PS8005
NAND Type	Mode	Support
SLC-SB	X1	X
	X2	X
SLC-LB	X1	O
	x2	O
MLC-SB	x1	X
	x2	X
MLC-LB (Conv.)	x1	O
	x2	O
MLC-LB (ABL)	x1	O
	x2	O
AG-AND	x1	X
	x2	X
TwinNAND	x1	X
	x2	X

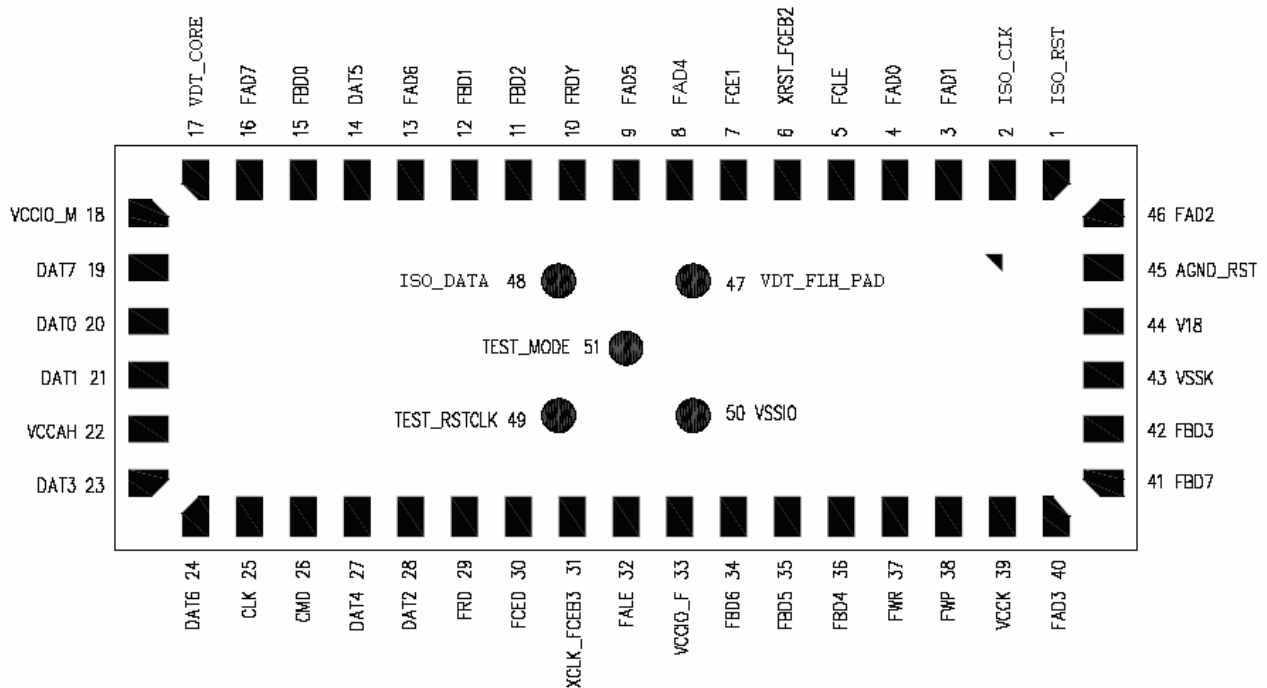
E. BLOCK DIAGRAM

SD CONTROLLER BLOCK DIAGRAM

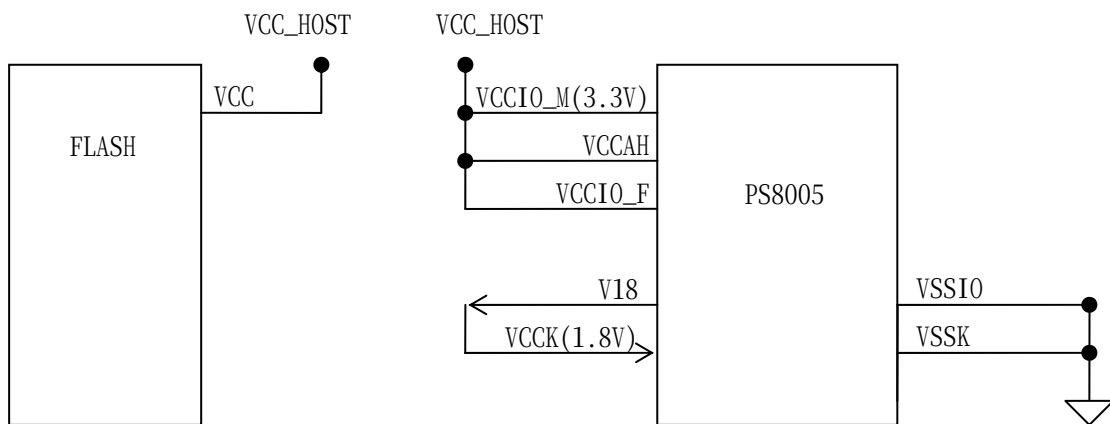


F. Pin Assignment and Description

PS8005 LGA Top View :



F1. Pin Description of Power Setting Diagram (flash voltage 2.7V ~ 3.6V)

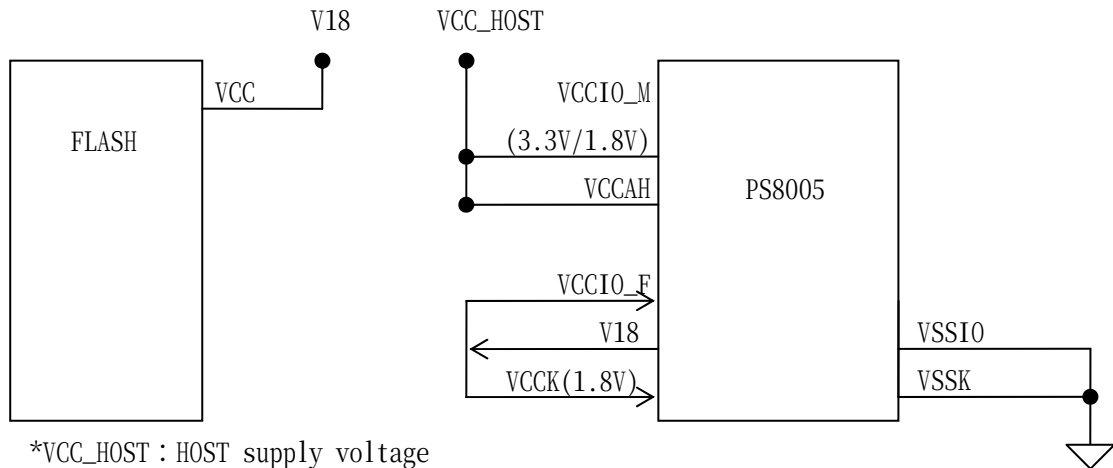


*VCC_HOST : HOST supply voltage

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F2. Pin Description of Power Setting Diagram (flash voltage 1.7V ~ 1.95V)



F3. Pins Listed in Numeric Order & Pin Description

Ball No.	Ball Name	Dir.	Description
1	ISO_RST	-	Don't care
2	ISO_CLK	-	Don't care
3	FAD1	I/O	Flash IO
4	FAD0	I/O	Flash IO
5	FCLE	O	Flash command latch enable
6	XRST_FCEB2	O	Flash chip enable
7	FCE1	O	Flash chip enable
8	FAD4	I/O	Flash IO
9	FAD5	I/O	Flash IO
10	FRDY	I	Flash ready/busy output
11	FBD2	I/O	Flash IO
12	FBD1	I/O	Flash IO
13	FAD6	I/O	Flash IO
14	DAT5	I/O	Data IO
15	FBD0	I/O	Flash IO
16	FAD7	I/O	Flash IO
17	VDT CORE	I	Test pin: Ground or floating
18	VCCIO_M	I	Power
19	DAT7	I/O	Data IO
20	DAT0	I/O	Data IO
21	DAT1	I/O	Data IO

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Ball No.	Ball Name	Dir.	Description
22	VCCAH	I	Power
23	DAT3	I/O	Data IO
24	DAT6	I/O	Data IO
25	CLK	I	Clock
26	CMD	I/O	Command / Response
27	DAT4	I/O	Data IO
28	DAT2	I/O	Data IO
29	FRD	O	Flash read enable
30	FCE0	O	Flash chip enable
31	XCLK_FCEB3	O	Flash chip enable
32	FALE	O	Flash address latch enable
33	VCCIO_F	I	Power
34	FBD6	I/O	Flash IO
35	FBD5	I/O	Flash IO
36	FBD4	I/O	Flash IO
37	FWR	O	Flash write enable
38	FWP	O	Flash write protect
39	VCCK	I	Power
40	FAD3	I/O	Flash IO
41	FBD7	I/O	Flash IO
42	FBD3	I/O	Flash IO
43	VSSK	I	Ground
44	V18	O	1.8v output
45	AGAND_RST	O	AGAND flash reset control
46	FAD2	I/O	Flash IO
47	VDT_FLH	I	Test pin: Ground or floating
48	ISO_DATA	-	Don't care
49	TEST_RSTCLK	I	Test pin: Ground or floating
50	VSSIO	I	Ground
51	TEST_MODE	I	Test pin: Ground or floating

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G. System Power Consumption

Table list as below is the power consumption of SD card with different type of flash memory. (PS8005 + Flash Memory)

Flash mode	Max Power up Current (uA)	Max Stand by Current (uA)	Max Read Current (mA)	Max Write Current (mA)
Single ⁽¹⁾ flash(1x8bit)	150	150	60@ 3.6V	60@ 3.6V
Parallel ⁽²⁾ flash(2x8bit)	200	200	80@ 3.6V	80@ 3.6V

(1)Data transfer mode is single channel.

(2)Data transfer mode is dual channel.

H. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	$V_{DD}-V_{SS}$	DC Power Supply	-0.3	+3.3	V
2	V_{IN}	Input Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	T_a	Operating Temperature	-25	+85	°C
4	T_{st}	Storage Temperature	-50	+125	°C

Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T_a	-25	+85	°C
V_{DD} Voltage	V_{DD}	2.7	3.6	V

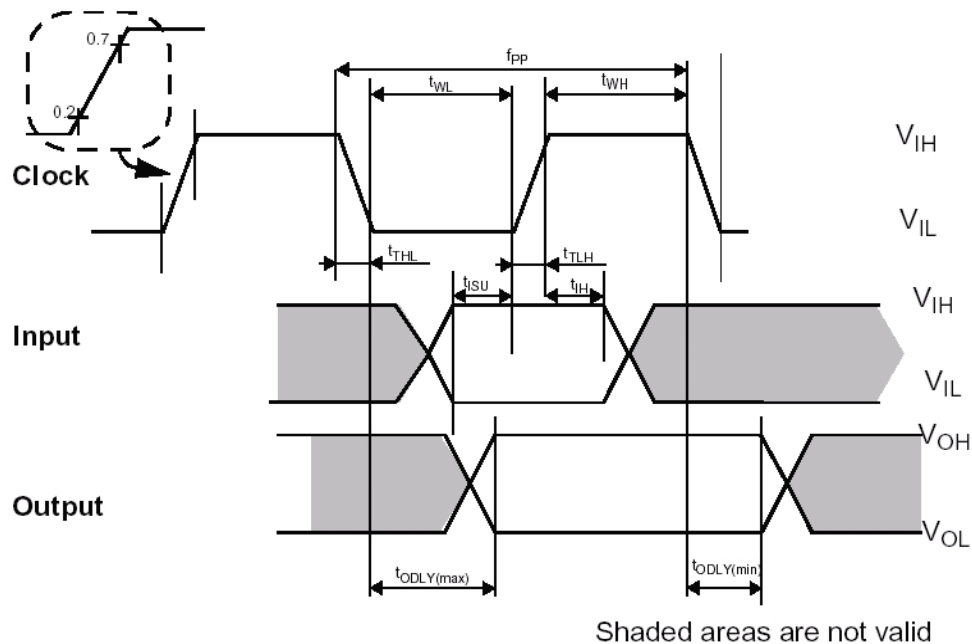
I. DC Characters

SD Controller DC Characteristics

Parameter	Symbol	Min.	Max	Unit	Condition
Output High Voltage	VOH	0.75*VDD		V	IOH=-100uA @VDD Min
Output Low Voltage	VOL		0.125*VDD	V	IOL=100uA @VDD Min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25*VDD	V	

J. AC Characters

J1. SD Interface timing



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Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_L \leq 100$ pF (7 cards)
Clock frequency Identification Mode(the low freq. is required for MultiMedia Card compatibility)	f_{OD}	0	400	KHz	$C_L \leq 250$ pF (21 cards)
Clock low time	t_{WL}	10		ns	$C_L \leq 100$ pF (7 cards)
Clock high time	t_{WH}	10		ns	$C_L \leq 100$ pF (7 cards)
Clock rise time	t_{TLH}		10	ns	$C_L \leq 100$ pF (7 cards)
Clock fall time	t_{THL}		10	ns	$C_L \leq 100$ pF (7 cards)
Clock low time	t_{WL}	50		ns	$C_L \leq 250$ pF (21 cards)
Clock high time	t_{WH}	50		ns	$C_L \leq 250$ pF (21 cards)
Clock rise time	t_{TLH}		50	ns	$C_L \leq 250$ pF (21 cards)
Clock fall time	t_{THL}		50	ns	$C_L \leq 250$ pF (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_L \leq 25$ pF (1 cards)
Input hold time	t_{IH}	5		ns	$C_L \leq 25$ pF (1 cards)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time	t_{ODLY}	0	14	ns	$C_L \leq 25$ pF (1 cards)

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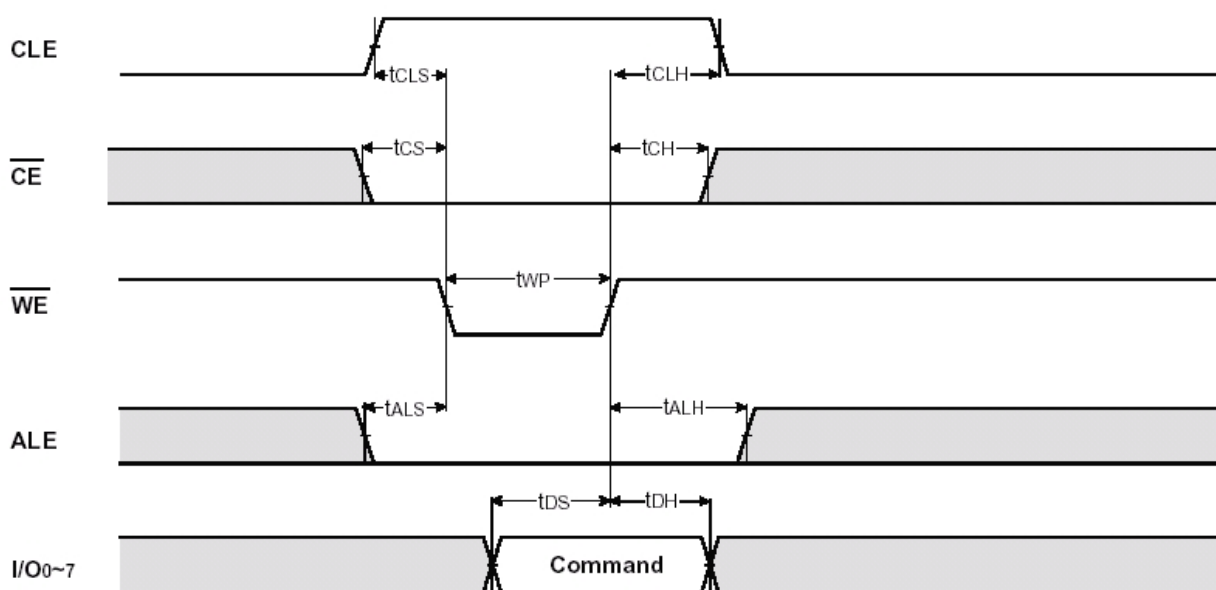
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J2. Flash Interface AC Characteristic

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	50	-	ns
CLE Hold Time	t_{CLH}	50	-	ns
/CE Setup Time	t_{CS}	200	-	ns
/CE Hold Time	t_{CH}	200	-	ns
WE Pulse Width	t_{WP}	30	50	ns
ALE Setup Time	t_{ALS}	50	-	ns
ALE Hold Time	t_{ALH}	50	-	ns
Data Setup Time	t_{DS}	20	50	ns
Data Hold Time	t_{DH}	30	100	ns
Write Cycle Time	t_{WC}	50	200	ns
WE High Hold Time	t_{WH}	20	150	ns
Read Cycle Time	t_{RC}	50	-	ns
/RE Pulse Width	t_{RP}	30	-	ns
/RE High Hold Time	t_{REH}	20	-	ns
Ready to /RE Low	t_{RR}	30	-	ns

J3. Flash memory timing

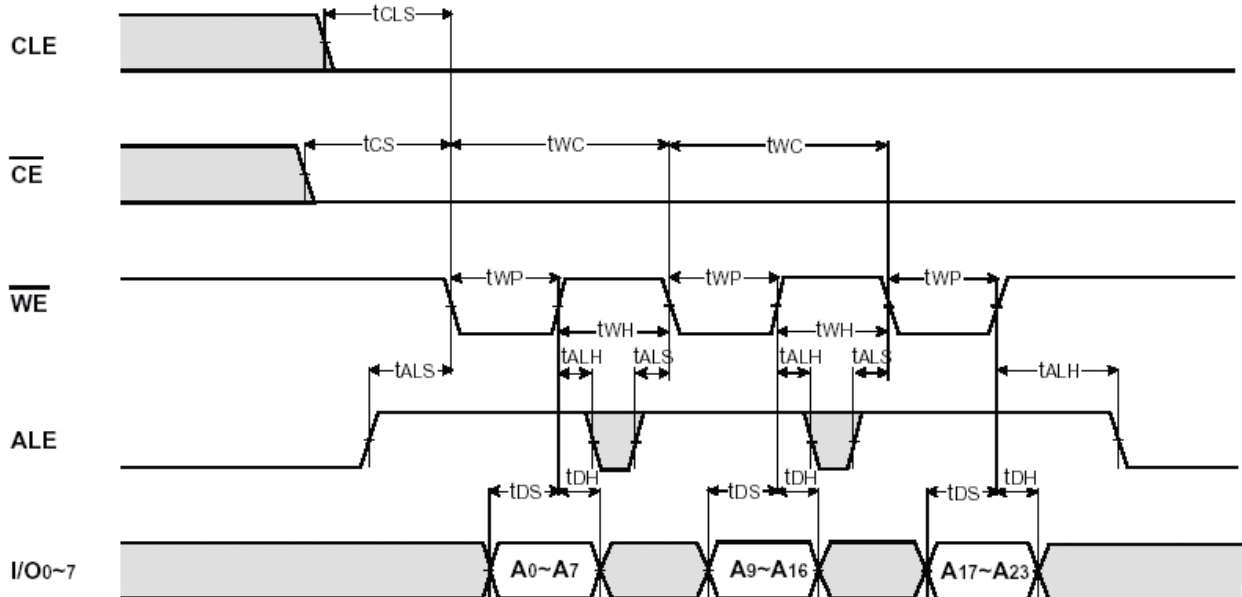
(a) Command Latch Cycle



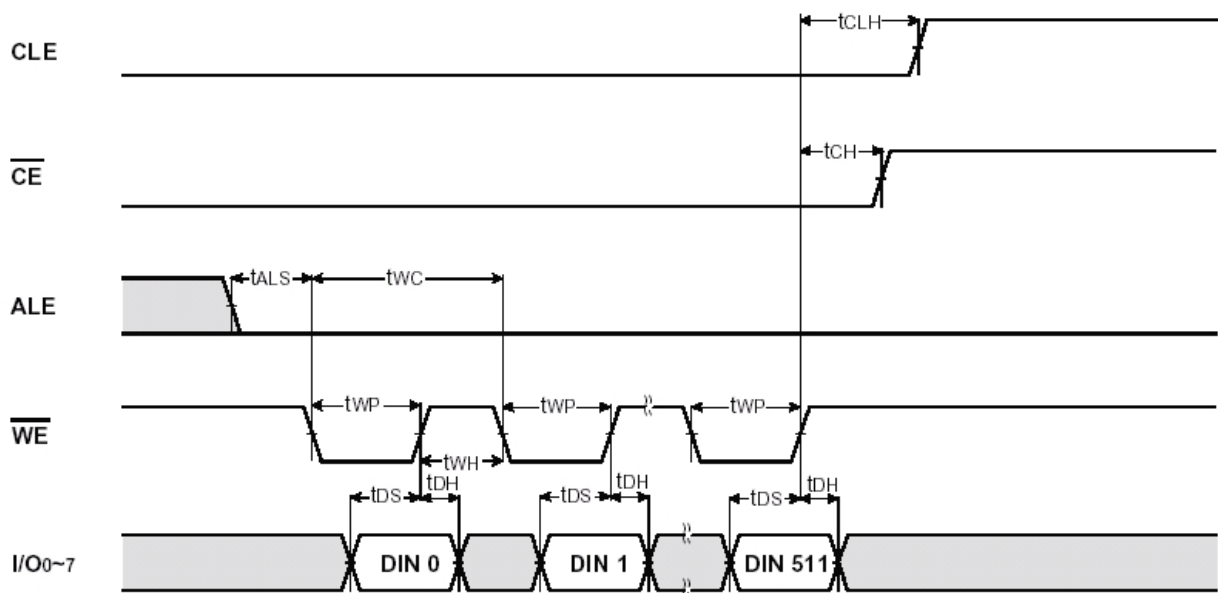
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(b) Address Latch Cycle



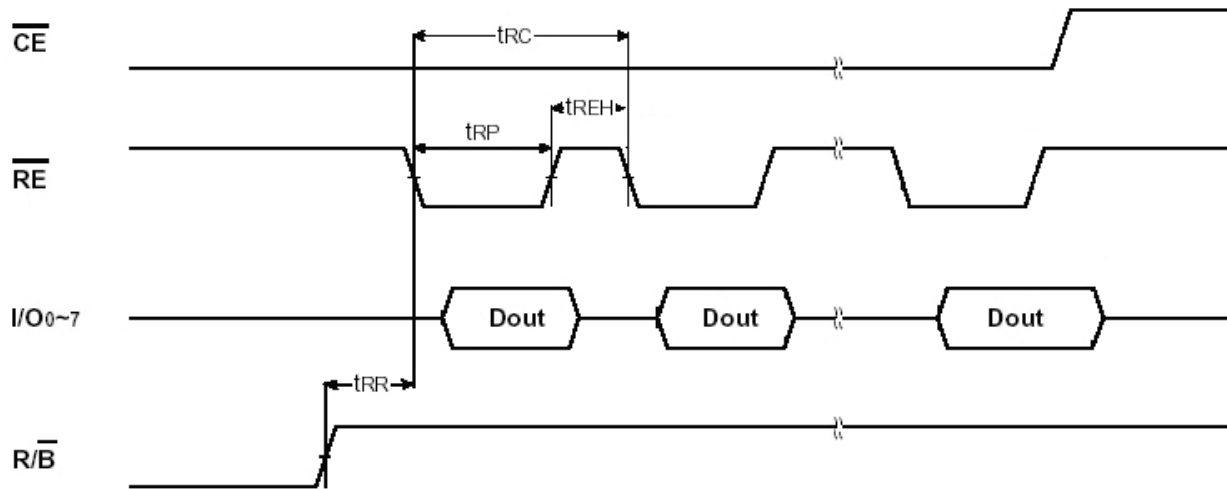
(c) Input Data Latch Cycle



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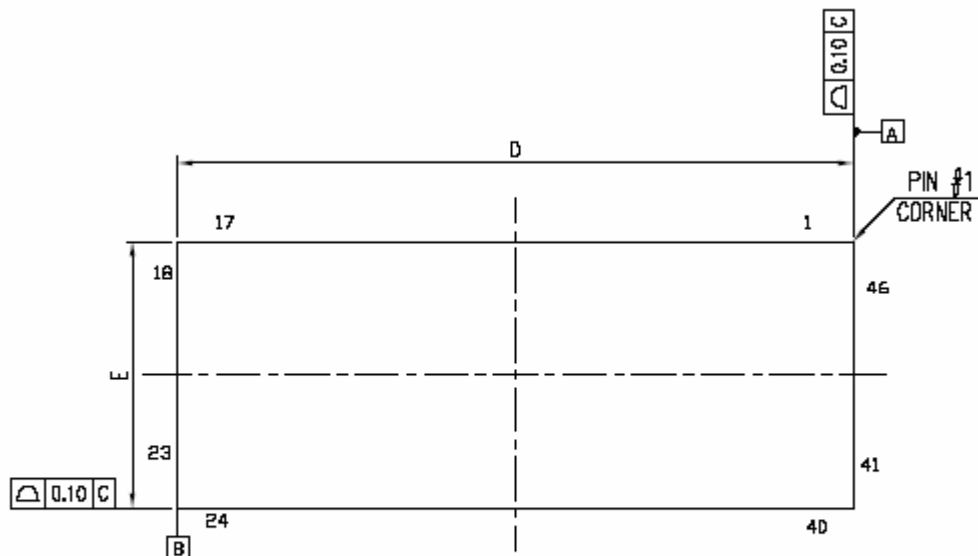
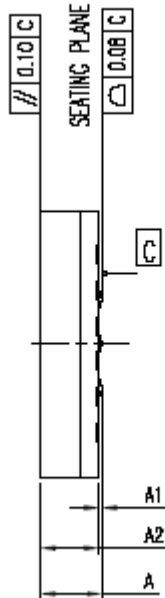
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(d) Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)



K. Package Information

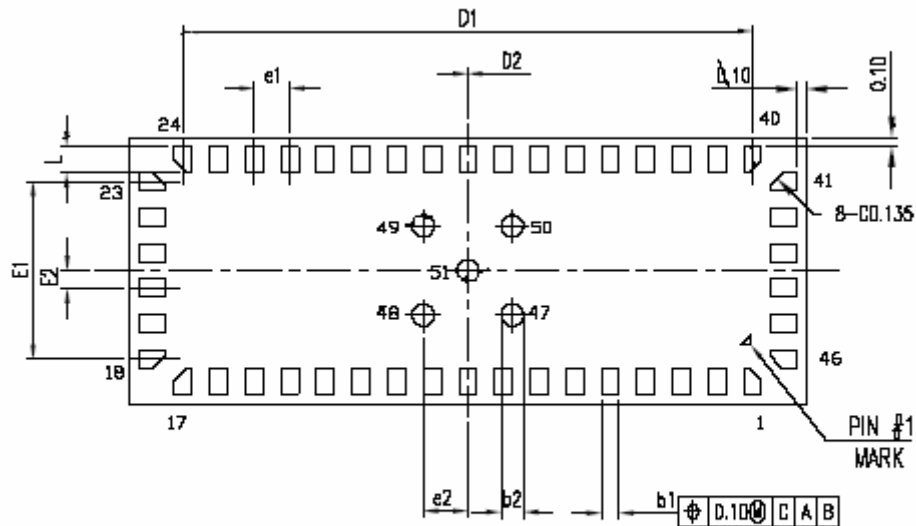
LGA 51 PIN (3.0 x 7.6 x 0.7 mm³)



TOP VIEW

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BOTTOM VIEW

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.60	0.69	0.77	24	27	30
A1	—	0.03	0.05	—	1	2
A2	0.60	0.66	0.72	24	26	28
b1	0.15	0.20	0.25	6	8	10
b2	0.20	0.25	0.30	8	10	12
D	7.50	7.60	7.70	295	299	303
D1	6.40 BSC.			252 BSC.		
D2	0.00 BSC.			0 BSC.		
E	2.90	3.00	3.10	114	118	122
E1	2.00 BSC.			79 BSC.		
E2	0.20 BSC.			8 BSC.		
e1	0.40 BSC.			16 BSC.		
e2	0.50 BSC.			20 BSC.		
L	0.25	0.30	0.35	10	12	14